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10/720,847	11/25/2003	Hajime Kimura	12732-181001 / US6768/692	3959

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EXAMINER	
PERVAN, MICHAEL	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/720,847	KIMURA, HAJIME	
	Examiner	Art Unit	
	Michael Pervan	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6-11,16,18-22,26-28 and 59-70* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-11,16,18-22,26-28 and 59-70* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/11/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 10 objected to because of the following informalities: "current drive circuit" should instead be –semiconductor device–. Appropriate correction is required.

Claim 18 objected to because of the following informalities: "the current source circuit" should instead be –a current source circuit–. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 6-11, 16, 18-22, 26-28 and 59-70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Knapp et al (US 6,373,454) in further view of Noboru et al (JP 2001-296873; as submitted by applicant).

In regards to claim 1, Knapp discloses a semiconductor device comprising:

a driven circuit comprising a first transistor (Fig. 2; transistor 30);

a signal line electrically connected to the first transistor through a node (Fig. 2; as can be seen from the drawing, the first transistor (30) is connected through a node (36) to a signal line).

Knapp does not disclose wherein a precharge voltage is supplied to the node through the signal line prior to supplying the signal current to the driven circuit.

Noboru discloses wherein a precharge voltage is supplied to the node through the signal line (paragraphs 14-15) prior to supplying the signal current to the driven circuit (paragraphs 14-15).

It would have been obvious at the time of invention to modify Knapp with the teachings of Noboru, precharge voltage being supplied to a node prior to supplying a signal current, because it would improve display characteristics since it would take less time to reach the display voltage because it has been precharged.

In regards to claim 2, Knapp does not disclose the semiconductor device according to claim 1,

wherein the first precharge circuit sets the precharge voltage to a potential equal to a potential of the node in a stationary state when the signal current is supplied to the driven circuit.

Noboru discloses the semiconductor device according to claim 1 wherein the first precharge circuit sets the precharge voltage to a potential equal to a potential of the node in a stationary state when the signal current is supplied to the driven circuit (paragraphs 14-15).

It would have been obvious at the time of invention to modify Knapp with the teachings of Noboru, precharge voltage being supplied to a node prior to supplying a signal current, because it would improve display characteristics since it would take less time to reach the display voltage because it has been precharged.

In regards to claim 3, Knapp does not disclose the semiconductor device according to claim 1,

wherein one of a plurality of voltages is selected as the precharge voltage.

Noboru discloses the semiconductor device according to claim 1 wherein one of a plurality of voltages is selected as the precharge voltage (paragraphs 14-15 and 18).

It would have been obvious at the time of invention to modify Knapp with the teachings of Noboru, precharge voltage being supplied to a node prior to supplying a signal current, because it would improve display characteristics since it would take less time to reach the display voltage because it has been precharged.

In regards to claims 6 and 60, Knapp and Noboru do not disclose the semiconductor device according to claim 1,

wherein the first precharge circuit comprises a second transistor (paragraph 15; first driving element (driving source 15) and second driving element (driving source 17)).

However, Noboru discloses first driving element (driving source 15) and second driving element (driving source 17) (paragraph 15).

Since, there is no benefit or advantage in the specification for having a second transistor, it would have been obvious to one of ordinary skill in the art at the time of invention to choose either a second transistor or first driving element and second driving element based on a designer's choice.

In regards to claim 7, Knapp and Noboru do not disclose the semiconductor device according to claim 1, further comprising

an impedance transformation amplifier.

However, Noboru discloses supplying a precharge voltage by pulse amplitude modulation (paragraph 18).

It would have been obvious to one of ordinary skill in the art at the time of invention to modify Noboru to supply the precharge voltage to the node and the signal line via an impedance transformation amplifier since impedance conversion for applying voltage is well known.

In regards to claim 8, Knapp and Noboru do not disclose the semiconductor device according to claim 3, further comprising

a second precharge circuit comprising a third transistor.

However, Noboru discloses a plural second setting means(paragraphs 14-15 and 18).

Since, there is no benefit or advantage in the specification for having a second precharge circuit with a third transistor, it would have been obvious to one of ordinary skill in the art at the time of invention to choose either a second precharge circuit with a third transistor or first driving element and second driving element based on a designer's choice.

In regards to claim 9, Knapp and Noboru does not disclose the semiconductor device according to claim 1,

wherein a precharge period T_b for supplying the precharge voltage to the node and the signal line is set so as to satisfy $T_b = R_L \times C_L$ based on a wiring resistance R_L and a parasitic capacitance C_L of the signal line.

However, Noboru discloses the time amount is changed to be proportional according to the magnitude of the signal current (paragraph 18).

Since, there is no benefit or advantage given in the specification as to choosing a precharge period T_b so as to satisfy $T_b = R_L \times C_L$, it would have been obvious to one of ordinary skill in the art at the time of invention to choose either time amount is changed to be proportional according to the magnitude of the signal current or a precharge period T_b so as to satisfy $T_b = R_L \times C_L$ based on a designer's choice.

In regards to claim 10, Knapp and Noboru does not disclose the semiconductor device according to claim 9, comprising:

wherein $T_a = T_b$ in a case where a supply period T_a of the signal current to the driven circuit satisfies $T_a < T_b$.

However, Noboru discloses the time amount is changed to be proportional according to the magnitude of the signal current (paragraph 18).

Since, there is no benefit or advantage given in the specification as to choosing a precharge period $T_a = T_b$ so as to satisfy $T_a < T_b$, it would have been obvious to one of ordinary skill in the art at the time of invention to choose either time amount is changed to be proportional according to the magnitude of the signal current or a precharge period $T_a = T_b$ so as to satisfy $T_a < T_b$ based on a designer's choice.

In regards to claims 11 and 61, Knapp discloses a semiconductor device according to claim 1, wherein:

the driven circuit is included in a pixel circuit (Fig. 1 and col. 5, lines 38-40); and

a power supply line is connected to the pixel circuit (Fig. 1 and col. 5, lines 38-40).

Knapp does not disclose the precharge circuit is included in a source driver circuit.

Noboru discloses the precharge circuit is included in a source driver circuit (Drawings 1-4).

It would have been obvious at the time of invention to modify Knapp with the teachings of Noboru, precharge circuit included in a source driver, because it would keep the pixel size small and reduce the overall size of the circuit because a separate precharge circuit would not be needed.

In regards to claim 16, Knapp and Noboru do not disclose the semiconductor device according to claim 6, wherein

the first and the second transistors are the same in size or in size according to it.

However, Noboru discloses first and second driving elements having sizes (Fig. 1).

Since, there is no benefit or advantage in the specification for having the first and second transistors being the same size, it would have been obvious to one of ordinary skill in the art at the time of invention to choose either the first and second transistors with the same size or the first and second driving element with the same size based on a designer's choice.

In regards to claim 18, Knapp discloses a semiconductor device comprising:

a driven circuit comprising a first transistor (Fig. 2; first transistor (30));

a first switch for controlling an electrical connection between the driven circuit and the precharge circuit (Fig. 2; first switch (33); and

a second switch for controlling a connection between the driven circuit and a current source circuit (Fig. 2; second switch (37)).

Knapp does not disclose a precharge circuit.

Noboru discloses a precharge circuit (paragraphs 14-18).

It would have been obvious at the time of invention to modify Knapp with the teachings of Noboru, a precharge circuit, because it would improve display characteristics since it would take less time to reach the display voltage because it has been precharged.

In regards to claim 19, Knapp discloses the semiconductor device according to claim 18, further comprising

a current source circuit for inputting a signal current to the driven circuit (Fig. 2; current source 35).

In regards to claim 20, Knapp discloses a semiconductor device comprising:

a driven circuit comprising a first transistor (Fig. 2; first transistor (30));

Knapp and Noboru do not disclose plural precharge circuits;

plural current source circuits for inputting a signal current to the driven circuit (paragraphs 14-18);

a first switch for controlling an electrical connection between the driven circuit and the plural precharge circuits;

a second switch for controlling an electrical connection between the driven circuit and the plural current source circuits.

However, Knapp discloses a semiconductor device comprising:

a current source circuit for inputting a signal current to the driven circuit (Fig. 2; current source 35).

a first switch for controlling an electrical connection between the driven circuit and the precharge circuit (Fig. 2; first switch (33); and

a second switch for controlling a connection between the driven circuit and a current source circuit (Fig. 2; second switch (37)).

Since, there is no benefit or advantage in the specification for having plural current source circuits, it would have been obvious to one of ordinary skill in the art at the time of invention to choose either plural current source circuits or a single current source circuit based on a designer's choice.

However, Noboru discloses a precharge circuit (paragraphs 14-18).

Since, there is no benefit or advantage in the specification for having plural precharge circuits, it would have been obvious to one of ordinary skill in the art at the time of invention to choose either plural precharge circuits or a single precharge circuit based on a designer's choice.

In regards to claims 21 and 59, Knapp and Noboru do not disclose the semiconductor device according to claim 20, further comprising

plural amplifier circuits for amplifying currents outputted from the plural precharge circuits.

However, Noboru discloses supplying a precharge voltage by pulse amplitude modulation (paragraph 18).

It would have been obvious to one of ordinary skill in the art at the time of invention to modify Noboru to supply the precharge voltage to the node and the signal line via an impedance transformation amplifier since impedance conversion for applying voltage is well known.

In regards to claim 22, Knapp and Noboru do not disclose the semiconductor device according to claim 18, wherein the precharge circuit comprises a second transistor.

However, Noboru discloses first driving element (driving source 15) and second driving element (driving source 17) (paragraph 15).

Since, there is no benefit or advantage in the specification for having a second transistor, it would have been obvious to one of ordinary skill in the art at the time of invention to choose either a second transistor or first driving element and second driving element based on a designer's choice.

In regards to claim 26, Knapp discloses the semiconductor device according to claim 19,

wherein the driven circuit is disposed in a pixel of a display device (Fig. 1 and col. 5, lines 38-40); and

the current source circuit is disposed in a source driver circuit (Figs. 1 and 2; the input line (35) is connected to the source driver which provides the current).

Knapp does not disclose the precharge circuit is disposed in a source driver circuit of the display device.

Noboru discloses the precharge circuit and the current source circuit are disposed in a source driver circuit of the display device (paragraph 14-18).

It would have been obvious at the time of invention to modify Knapp with the teachings of Noboru, precharge circuit included in a source driver, because it would keep the pixel size small and reduce the overall size of the circuit because a separate precharge circuit would not be needed.

In regards to claims 27 and 62, Knapp and Noboru do not disclose the semiconductor device according to claim 19,

wherein the driven circuit is disposed in a digital voltage/analog current conversion circuit; and

the precharge circuit and the current source circuit are disposed in a reference current source circuit.

However, Knapp discloses wherein the driven circuit is disposed in a pixel of a display device (Fig. 1 and col. 5, lines 38-40) and the current source circuit is disposed in a source driver circuit (Figs. 1 and 2; the input line (35) is connected to the source driver which provides the current).

Since, there is no benefit or advantage given in the specification for choosing to have the driven circuit disposed in a reference current source circuit instead of a pixel and the current source in a reference current source circuit instead of a source driver, it would have been obvious to one of ordinary skill in the art to choose either having

driven circuit disposed in a reference current source circuit or a pixel and the current source disposed in a reference current source circuit or a source driver based on a designer's choice.

However, Noboru discloses the precharge circuit disposed in source driver circuit (paragraph 14-18).

Since, there is no benefit or advantage given in the specification for choosing to have the precharge circuit disposed in a reference current source circuit instead of a source driver circuit, it would have been obvious to one of ordinary skill in the art to choose either having precharge circuit disposed in a reference current source circuit or a source driver circuit based on a designer's choice.

In regards to claims 28 and 63, Knapp and Noboru do not disclose the semiconductor device according to claim 22,

wherein a gate and a drain of the second transistor are connected to each other.

However, Noboru discloses the precharge circuit comprising a switch (Fig. 1).

Since, there is no benefit or advantage in the specification for choosing a transistor instead of a switch, it would have been obvious to one of ordinary skill in the art at the time of invention to choose a precharge circuit comprising either a transistor or a switch based on a designer's choice.

In regards to claims 64-66, Knapp and Noboru do not disclose the amplifier is a source follower circuit.

Noboru discloses supplying a precharge voltage by pulse amplitude modulation (paragraph 18).

Since there is no benefit or advantage in the specification for choosing an amplifier circuit to be a source follower circuit, it would have been obvious to one of ordinary skill in the art at the time of invention to choose an amplifier circuit to be a source follower circuit based on a designer's choice because a source follower circuit is one type of amplifier circuit.

In regards to claims 67-70, Knapp and Noboru disclose wherein the second transistor is connected to the first switch through a wiring (Fig. 2; as can be seen from the drawing, the switch (33) is connected to the second transistor (of Noboru) by a wiring).

Response to Arguments

4. Applicant's arguments with respect to claims 1-3, 6-11, 16, 18-22, 26-28 and 59-70 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Pervan whose telephone number is (571) 272-0910. The examiner can normally be reached on Monday - Friday between 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MVP
Oct. 25, 2007

AMR A. AWAD
SUPERVISORY PATENT EXAMINER